In the specification:

On page 1, delete line 1.

On page 1, replace the title with --RECOVERING CLOCK AND FRAME INFORMATION FROM DATA STREAM--

On page 1, line 6, insert:

--RELATED APPLICATIONS

This application claims the benefit of the priority date of German application DE 102.28.574.8, filed on June 26, 2002, the contents of which are herein incorporated by reference.

FIELD OF INVENTION--

On page 1, line 13, insert the header --BACKGROUND--

Replace the paragraph beginning on page 1, line 28 with the following:

--~~Said~~ The data ~~block~~ clock is necessary, for example, ~~in order~~ to synchronize a PLL, to output a data stream in data stream units or data blocks, and to reliably receive corresponding data streams.--

On page 2, line 8, insert the header --SUMMARY--

On page 2, delete the paragraph beginning on line 17.

On page 2, delete the paragraph beginning on line 20.

On page 4, delete the paragraph beginning on line 16.

On page 6, line 15, insert the header --BRIEF DESCRIPTION OF THE DRAWINGS--

On page 6, line 33, insert the header --DETAILED DESCRIPTION--

Replace the paragraph beginning on page 6, line 34 with the following new paragraph

--Figure 1 shows the basic construction of a digital data stream, the data stream being subdivided into superframes 106a-106n, on the one hand, and data frames 101a-101n, on the other hand. The data frames 101a-101n have a structure as will be described below with reference to Figure 4. Figure 1 serves merely as an example for illusterating a possible structure of digital data stream 100, ~~[lacuna]~~ which is received by means of a data stream receiver 200, described below with reference to Figure 2.--

Replace the paragraph beginning on page 8, line 10, with the following new paragraph:

--Furthermore, the data clock determination unit 202 is connected to a frame detection unit 206, which detects a start of a frame, i.e. a frame start 110, by detecting a specified number of dummy bits. In this case, a frame start 110 of the at least one data frame 101 is defined by a frame synchronization word 104 or by synchronization bits in the data stream unit 108 when the frame synchronization word 104 is preceded by at least ~~N [sic] =~~ N+K+1 dummy bits. In the exemplary embodiment according to the invention, the dummy bits are provided as logic ones "1". A frame start 110 detected in this way is finally output from the frame detection unit 206. --